DESIGN CHALLENGES FOR SCALABLE CONCURRENT DATA STRUCTURES for Many-Core Processors

DIMACS
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Data Structures In Manycore Sys.

- Decomposition
- Load Balancing
- Inter Task Communication
- Synchronization
Concurrent Data Structures: Our NOBLE Library project

- Fundamental shared data structures
  - Stacks
  - Queues
  - Deques
  - Priority Queues
- Memory Management
  - Memory allocation
  - Memory reclamation (garbage collection)
- Atomic primitives
  - Single-word and Multi-word transactions.
Many-core?

- No clear definition, but at least **more than 10 cores**
- Some say thousands

```
Dual-, Quad-, Hexa-, Octo-, Dekaexi - Trianta - Many-core!
```

- The most commonly available many-core platforms are the medium to high end graphics processors
- Have up to 30 multiprocessors and available at a low-cost
- **CUDA** and **OpenCL** have made them easily accessible
# A Basic Comparison

<table>
<thead>
<tr>
<th>Normal processors</th>
<th>Graphics processors</th>
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<tbody>
<tr>
<td>Large cache</td>
<td>Small/No cache</td>
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<td>SIMD</td>
</tr>
<tr>
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<td>Wide and fast memory bus with memory operations that can be coalesced</td>
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CUDA System Model

Global Memory

Multiprocessor 0
- Thread Block 0
- Thread Block 1
- Shared Memory

Multiprocessor 1
- Thread Block x
- Thread Block y
- Shared Memory
CUDA System Model

- Atomic primitives
  - None -> For global memory -> For shared memory
- Threads per multiprocessor
  - 768 -> 1024 -> 1536
- Shared memory
  - 16KB -> 48KB
- SIMD width
  - 8 words -> 32 words
Locks are not supported

- Not in CUDA, not in OpenCL
  - **Fairness** of hardware scheduler **unknown**
  - Thread block holding a lock might be swapped out **indefinitely**, for example
No Fairness Guarantees

...  
...

while(atomicCAS(&lock,0,1));
ctr++;
lock = 0;

Thread holding lock is never scheduled!
Lock-free Data Structures

- Mutual exclusion (Semaphores, mutexes, spin-locks, disabling interrupts: Protects critical sections)
  - Locks limits concurrency, priority inversion
  - Busy waiting – repeated checks to see if lock has been released or not
  - Convoying – processes stack up before locks
  - **Blocking Locks are not composable**
    - All code that accesses a piece of shared state must know and obey the locking convention, regardless of who wrote the code or where it resides.

- Lock-freedom is a **progress guarantee**
- In practice it means that
  - A fast process doesn’t have to wait for a slow or dead process
  - No deadlocks
- Shown to **scale better** than blocking approaches

**Definition**
For all possible executions, at least one concurrent operation will succeed in a finite number of its own steps.
In this case a non-blocking design is easy:

```java
class Counter {
    int next = 0;

    int getNumber () {
        int t;
        do {
            t = next;
        } while (CAS (&next, t, t + 1) != t);
        return t;
    }
}
```

Atomic compare and swap

Location

Expected value

New value
Lock Free Concurrent Data Structures

Doubly Linked Lists

Hashtables, Dictionaries

Skiplists

Queues, Priority, Deques

LF DS in Normal Processors:
Joint work with D. Cederman,
A. Gidenstamn, Ph. Ha, M.
Papatriantafilou, H. Sundell, Y.
Zhang

Graphics Processors:
Joint work D. Cederman, Ph.
Ha, O. Anshus
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Lock-free Data Structures Without Atomics?

Emulating CAS from Coalesced Memory Access
Coalesced Global Memory Accesses

• The simultaneous global memory accesses by each thread of a half-warp during the execution of a single read or write instruction will be coalesced into a single access if:
  - The size of the memory element accessed by each thread is either 4, 8, or 16 bytes
  - The elements form a contiguous block of memory
  - The $N^{th}$ element is accessed by the $N^{th}$ thread in the half-warp
  - The address of the first element is aligned to 16 times the element’s size

• Coalescing happens even if some threads do not access memory (divergent warp)
Aligned-inconsecutive word (aiword)

- Memory is aligned to $m$-unit words, $m$ is a constant.
  - $m$-aiword for short

- A read/write operation accesses an arbitrary non-empty subset of the $m$ units of an aiword.
  - $m$-aiwrite = $m$-aiword assignment.

- Alignment restriction
  - $m$-aiwords must start at addresses that are multiples of $m$.

- Ex: 8-aiwrite
$m$-aiword’s consensus no. $\geq \left\lfloor \frac{m+1}{2} \right\rfloor$

- **Idea:**
  - Construct a *binary* consensus object for $N=\left\lfloor \frac{m+1}{2} \right\rfloor$ processes in which $(N-1)$ processes propose the same value.
  - Construct a *multivalued* consensus object for $N$ processes using the binary consensus object.

- **Ex: 9-aiword**

*Binary consensus (BC) for 4+1 processes*

Consensus for 5 processes

- $[0, 4, 8] \Rightarrow p_4 \rightarrow p_0$
- $[1, 5, 8] \Rightarrow p_1 \rightarrow p_4$
- $[2, 6, 8] \Rightarrow p_4 \rightarrow p_2$
- $[3, 7, 8] \Rightarrow p_4 \rightarrow p_3$

$\Rightarrow$ red wrote first
Hardware Primitives are Significant for Concurrent Data Structures

![Graph showing the comparison between CAS and MemAcc over varying threads. CAS shows a linear increase in time as the number of threads increases, while MemAcc remains constant.](image-url)
Concurrent Data Structures Need Scalable Strong Synchronization Primitives

Desired Features

- Scalable
- Universal
  - powerful enough to support any kind of synchronization (like CAS, LL/SC)
- Feasible
  - Easy to implement in hardware
- Easy-to-use in Algorithmic Design
Non-blocking Full/Empty Bit

Joined work with Phuong Ha and Otto Anshus
Non-blocking Full/Empty Bit

- Combinable operations
- Universal
- Feasible
  - Slight modification of a primitive that has been implemented in hardware
- Easy-to-use
A variant of the original FEB that always returns a value instead of waiting for a conditional flag

Test-Flag-and-Set
TFAS( x, v) {
    (o, flag_o) ← (x, flag_x);
    if flag_x = false then
        (x, flag_x) ← (v, true);
    end if
    return (o, flag_o);
}

Original FEB: Store-if-
Clear-and-Set
SICAS(x,v) {
    Wait for flag_x to be false;
    (x, flag_x) ← (v, true);
}
A variant of the original FEB that always returns a value instead of waiting for a conditional flag

Test-Flag-and-Set
\[
\text{TFAS}(x, v) \{ \\
    (o, flag_o) \leftarrow (x, \text{flag}_x); \\
    \text{if flag}_x = \text{false} \text{ then} \\
    \quad (x, \text{flag}_x) \leftarrow (v, \text{true}); \\
    \quad \text{end if} \\
    \quad \text{return } (o, \text{flag}_o); \\
\} 
\]

Store-And-Clear
\[
\text{SAC}(x, v) \{ \\
    (o, flag_o) \leftarrow (x, \text{flag}_x); \\
    (x, \text{flag}_x) \leftarrow (v, \text{false}); \\
    \quad \text{return } (o, \text{flag}_o); \\
\} 
\]

Store-And-Set
\[
\text{SAS}(x, v) \{ \\
    (o, flag_o) \leftarrow (x, \text{flag}_x); \\
    (x, \text{flag}_x) \leftarrow (v, \text{true}); \\
    \quad \text{return } (o, \text{flag}_o); \\
\} 
\]

Load
\[
\text{Load}(x) \{ \\
    \text{return } (x, \text{flag}_x); \\
\} 
\]
Key idea: Combinability

⇒ eliminates contention & reduce load

Ex: TFAS

Note: CAS or LL/SC is not combinable
New algorithmic techniques that come from the introduction of new hardware features.

Core algorithmic design did not change when going from GP CPU to GPU.

Optimistic concurrency control works in manycore systems. Hard to derive worst case guarantees.

Scheduler part of the reference model?

Need to start a discussion with the architects about the abstractions/primitives that we want/need.
PEPPHER: PERFORMANCE PORTABILITY AND PROGRAMMABILITY FOR HETEROGENEOUS MANY-CORE ARCHITECTURES
Project Consortium

- University of Vienna (Coordinator), Austria
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- Chalmers University, Sweden
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- Codeplay Software Ltd., UK
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- INRIA, France
  - Raymond Namyst
- Intel GmbH, Germany
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- Linköping University, Sweden
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- Movidius Ltd. Ireland
  - David Moloney
- Karlsruhe Institute of Technology, Germany
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Thank You!